Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1 and add new claims 55-85 as follows:

Listing of Claims:

1-54. (Cancelled)

55. (New) A method of masking data being written to a memory device during a write partial mode, the memory device including data, control, and address busses, the method comprising:

receiving data words and data masking words on the data bus,

storing at least one of the data masking words and at least one of the data words,

applying at least one of the stored data masking words to mask at least one of the stored data words thereby producing at least one masked data word;

applying at least one masked data word to the memory-cell array.

56. (New) The method of claim 55 wherein the data words on the data bus are stored in the memory device prior to applying the data masking words to the data words.

57. (New) The method of claim 55 wherein the data masking word includes masking data for masking and not masking corresponding segments of data contained in the data words.

58. (New) The method of claim 57 wherein at least one of the segment comprises a byte of data.

59. (New) The method of claim 55 further comprising

receiving and storing at least one data word over the data bus during a write mode;

applying the at least one data word to the memory-cell array.

60. (New) A read/write circuit adapted to receive data words and data masking words on a data bus, the read/write circuit operable during a write-partial mode to store at least one data masking word and at least one data word applied on the data bus, and operable to apply the at least one data masking word to mask the at least one data word and to thereafter apply the at least one data word to the memory-cell array.

61. (New) The read/write circuit of claim 60 wherein the data masking word includes masking data for masking and not masking corresponding segments of data contained in the data words.

62. (New) The read/write circuit of claim 61 wherein at least one of the segments comprises a byte of data.

63. (New) The read/write circuit of claim 60 wherein the read/write circuit receives all data masking words prior to receiving the data words.

64. (New) The read/write circuit of claim 60 wherein the read/write circuit is further operable during a write mode to receive and store at least one data word over the data bus and apply the at least one data word to the memory-cell array.

65. (New) The read/write circuit of claim 64 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

66. (New) The read/write circuit of claim 65 wherein at least one of the data words in the burst are stored in read/write circuit prior to the read/write circuit applying the data masking word to mask the at least one of the stored data words.

67. (New) A read/write circuit adapted to receive data words and data masking words applied on a data bus, and operable during a write mode to store data words applied on the data bus and apply the data words to the memory-cell array, and operable during a write-partial mode to store at least one data masking word and at least one data word applied on the data bus, and operable to apply masking data contained in at least one of the data masking words to selectively mask and not mask data contained in at least one of the data words, and to thereafter apply the masked and not masked data to the memory-cell array.

68. (New) The read/write circuit of claim 67 wherein the data masking word includes masking data for masking and not masking corresponding segments of data contained in the data words.

69. (New) The read/write circuit of claim 67 wherein at least one of the segments comprises a byte of data.

70. (New) The read/write circuit of claim 67 wherein the read/write circuit receives all data masking words prior to receiving the data words.

71. (New) The read/write circuit of claim 67 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

72. (New) The read/write circuit of claim 67 wherein during the write-partial mode of operation all data words in the burst are stored in read/write circuit prior to the read/write circuit applying the data masking word to mask the data words.

73. (New) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder and control circuit;

a read/write circuit coupled to the data bus and the memory-cell array, the read/write circuit operable during a write-partial mode to receive at least one data masking word and at least one data word applied on the data bus and store the received words, and operable to apply the at least one data masking word to mask at least one of the data words and to thereafter apply at least one of the masked data words to the memory-cell array.

74. (New) The memory device of claim 73 wherein the memory comprises a double-data rate synchronous dynamic random access memory.

75. (New) The memory device of claim 73 wherein the read/write circuit receives all data masking words prior to receiving the data words.

76. (New) The memory device of claim 73 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

77. (New) The memory device of claim 73 wherein all data words in the burst are stored in the read/write circuit prior to the read/write circuit applying the data masking word to mask the data words.

78. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder and control circuit;

a read/write circuit coupled to the data bus and the memory-cell array, the read/write circuit operable during a write-partial mode to receive at least one data masking word and at least one data word on the data bus and store the received words, and operable to apply the at least one data masking word to mask at least of the data words and to thereafter apply at least one of the masked data word to the memory-cell array.

79. (New) The computer system of claim 78 wherein the memory comprises a double-data rate synchronous dynamic random access memory.

80. (New) The computer system of claim 78 wherein the read/write circuit receives all data masking words prior to receiving the data words.

81. (New) The computer system of claim 78 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

82. (New) The computer system of claim 27 wherein all data words in the burst are stored in the read/write circuit prior to the read/write circuit applying the data masking word to mask the data words.

83. (New) A method of masking data being written to a memory device, the memory device including a data bus, the method comprising:

applying masking data on the data bus;

storing the masking data in the memory device;

applying write data on the data bus;

storing the write data in the memory device; and

applying the stored masking data to mask the stored write data.

84. (New) The method of claim 83 wherein applying masking data on the data bus and storing the masking data in the memory device occur before applying write data on the data bus and storing the write data in the memory device.

85. (New) The method of claim 83 wherein applying masking data on the data bus comprises applying a single data word on the data bus.